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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,272	04/10/2001	Kirk Prall	3969.3US (95-0310.3)	2827

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EXAMINER
WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,272	PRALL ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Preliminary Amendment filed on July 23, 2001.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez et al. (US 5,323,038) in view of Osaki et al. (US 5,565,708).

Gonzalez et al. Shows (fig. 12) a dynamic random access memory array (DRAM) comprising a substrate (52), a plurality of memory cells, each cell having field effect access transistors and a stacked capacitor (96). The field effect transistors have source/drain regions (80-right) that function as storage node junctions and are connected to the capacitor of the memory cell. The transistors also have second source/drain regions (80-left) which functions as an access node junction and an insulated gate overlying the substrate. The gate is insulated from the substrate by a gate dielectric (60) of silicon oxide and has vertical sidewalls (74 & 78) and an upper surface (66) which are both covered by a dielectric of nitride. The gate electrode (62) comprises dope polysilicon and a silicide (64) cap layer. Along the length of the substrate, other access transistors are insulated from the substrate by a field oxide region (54). An interlevel dielectric layer (98) comprising a second dielectric material is

blanketed over the substrate to a level above the capacitors. A plurality of digit line contact openings (100) penetrate the interlevel dielectric layer and terminate at an access node junction. The contact opening is lined with titanium nitride (102) and tungsten fills the remainder of the opening to form a tungsten plug (104). A digit line is formed on top of the interlevel dielectric layer and makes electrical contact to the tungsten plug. Gonzalez shows all of the elements of the claims except the digit line contact opening having the additional titanium metal layer on the sidewalls of the opening and the silicide layer formed on the access node junction. Ohsaki et al. shows (figs. 14 and 15) a contact structure of a memory array comprising a contact opening formed in an interlayer dielectric layer (53). An access node junction (52) has a layer of silicide (57) formed on it. A layer of titanium (55) is formed on the sidewalls of the opening. A titanium nitride layer (56) and CVD tungsten (59) are subsequently deposited to fill the openings (col. 1, line 60-col. 2, line 20). The silicide layer is formed by reacting the titanium with the source/drain region (col.1, lines 62-67). As can be seen from the figure, the titanium layer is overlying the silicide layer by does not make contact with the tungsten layer. The titanium/titanium nitride combination in conjunction with the silicide layer provides a low resistance electrical contact reduces junction defects. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the contact opening of Gonzalez by adding a titanium metal layer and silicide to the access node junction of a transistor because Ohsaki et al. teaches that such configuration provides a low resistance electrical connection and reduce junction defects.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harada et al. (US 5,712,509), Chen (US 5,525,543), Ema (US 5,561,623), and Sakamoto (JP 5-47704 A) also show semiconductor memory devices having titanium and tungsten filled contact structures. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

February 10, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800